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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,124	03/18/2004	Kuilong Wang	IDT-1875	8908

7590 06/28/2005

Glass & Associates
PO Box 1220
Los Gatos, CA 95031-1220

EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/805,124	WANG ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,16,17 and 20* is/are rejected.

7)☒ Claim(s) *11-15,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/18/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 031804
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 is objected to because of the following informalities: at line 18, the term " anti reflective " should be -- anti-reflective --.

2. Claim 16 is objected to because of the following informalities: at line 16, the term " said gate film stack " should be – said single gate stack --.

3. Claim 12 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The terms "said first mask" and " said second mask" are not previously recited in the base claim 10.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 14, it recites "said dielectric film **only** extending with said **first** region" (line 15), which is contradicting with the limitation recited in the base claim 7, in which it recites "a dielectric layer that extends **within said first** region **and within said second** region" (line 17). (emphasis added)

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1-4, 7-9, 16, 17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dobuzinsky et al. (US 6,518,151).

In re claim 1, Dobuzinsky et al. teach a method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

- forming a dielectric layer 11 that extends within said first region (i.e. DRAM array region) and within said second region (i.e. logic circuit region) (Fig.4);
- forming a gate film stack 11/12/40/50 that extends within said first region and within said second region, said gate film stack immediately overlying said dielectric layer 11 (Fig.5); and
- patterning said gate film stack 11/12/40/50 to define gate structures 90 in said first region and in said second region (Fig.9).

In re claim 2, Dobuzinsky et al teach that the gate film stack 11/12/40/50 is a single gate film stack that extends, at the same time within both said first region and said second region, said

patterning said gate film stack 11/12/40/50 so as to define gate structures 90 within said first region and said second region (Fig.9).

In re claim 3, Dobuzinsky et al teach forming self-aligned contacts 120 that coupled to said gate structures 90 in said first region; and forming self-aligned contacts 120 that coupled to source and drain regions in said first region (Fig.12).

In re claim 4, Dobuzinsky et al teach that said gate film stack 11/12/40/50 comprises a gate layer 12, and a dielectric film 40/50, said dielectric film 40/50 including a dielectric hardmask layer 40 and an antireflective coating 50 (Fig.5).

In re claim 7, Dobuzinsky et al. teach a method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

- forming a dielectric layer 11 that extends within said first region (i.e. DRAM array region) and within said second region (i.e. logic circuit region) (Fig.4);
- forming a gate film stack 11/12/40/50 that includes a gate layer 12 and that includes a dielectric film 40/50 overlies said gate layer 12, said gate film stack 11/12/40/50 extending within said first region and within said second region (Fig.5); and
- patterning said gate film stack 11/12/40/50 to define gate structures 90 in said first region and in said second region (Fig.9).

In re claim 8, Dobuzinsky et al teach that the gate film stack 11/12/40/50 is a single gate film stack that extends, at the same time, within both said first region and said second region, said patterning said dielectric layer 40/50 and said gate film stack 11/12/40/50 removing portions of said gate film stack 11/12/40/50 and said dielectric 40/50 (Fig.6).

In re claim 9, Dobuzinsky et al teach that the gate film stack is thicker in said first region (i.e. the DRAM array region) than in said second region (i.e. the logic circuit region) (Fig.9).

In re claim 16, Dobuzinsky et al. teach a method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

- forming a dielectric layer 11 that extends within said first region (i.e. DRAM array region) and within said second region (i.e. logic circuit region) (Fig.4);
- forming a single gate film stack 11/12/40/50 that includes a gate layer 12 and that includes a dielectric film 40/50 overlies said gate layer 12, said gate film stack 11/12/40/50 extending within said first region and within said second region (Fig.5); and
- patterning said single gate film stack 11/12/40/50 to define gate structures 90 in said first region and in said second region (Fig.9).

In re claim 17, Dobuzinsky et al teach that said dielectric film 40/50 including a dielectric hardmask layer 40 and an antireflective coating 50 (Fig.5).

In re claim 20, Dobuzinsky et al teach an integrated circuit device having self-aligned devices and non-self-aligned contact devices, said integrated circuit device formed in accordance with the method of claim 17.

8. Claim 1, 5, 6, 7, 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Adetutu et al. (US 6,790,719).

In re claim 1, Adetutu et al. teach a method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

- forming a dielectric layer 14 that extends within said first region 39 and within said second region 37 (Fig.2);
- forming a gate film stack 16/18/20/22 (Fig.1) that extends within said first region 39 and within said second region 37, said gate film stack 16/18/20/22 immediately overlying said dielectric layer 14 (Fig.1); and
- patterning said gate film stack 16/18/20/22 to define gate structures 37 and 39 in said first region and in said second region (Fig.2).

In re claim 5, Adetutu et al. teach that only N-type semiconductor devices 40 (col. 4, line 1) are formed within said first region 39 (Fig.4) and wherein both N-type devices and P-type devices are formed in said second region.

In re claim 6, Adetutu et al teach an integrated circuit device having self-aligned devices and non-self-aligned contact devices, said integrated circuit device formed in accordance with the method of claim 5.

In re claim 7, Adetutu et al. teach a method for forming self-aligned contact devices in a first region of a semiconductor substrate and non-self-aligned contact devices in a second region of said semiconductor substrate comprising:

- forming a dielectric layer 14 that extends within said first region 39 and within said second region 37 (Fig.2);

- forming a gate film stack 16/18/20/22 that includes a gate layer 20 and that includes a dielectric film 22 overlies said gate layer 20, said gate film stack 16/18/20/22 extending within said first region and within said second region (Fig. 1); and
- patterning said gate film stack 16/18/20/22 to define gate structures 37 and 39 in said first region and in said second region (Fig.2).

In re claim 9, Adetutu et al. teach that the gate film stack is thicker in said first region 38 than in said second region 40 (Fig.4).

In re claim 10, Adetutu et al. teach that said gate layer comprises polycide 54 and 68,said patterning said gate film stack forming polycide lines 52 and 64 that extends between said first region and said second region (Fig.4).

Allowable Subject Matter

9. Claims 11-15 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record at least neither teaches nor suggests using first etch mask and a second etch mask, wherein the first etch mask covering portions of said first region and most of said second region and said second etch mask covering all of said first region and portions of said second region (claim 11); first (etch) mask and second (etch) mask overlap to form a broadened region along lines that cross between the first(etch) mask and second (etch) mask (claim 12); and performing a first selective etch and performing a second selective etch (claim14).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

June 25, 2005

HSIEN-MING LEE
PRIMARY EXAMINER